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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/666,669	09/19/2003	Tim Tuan	X-1462 US	8241

24309 7590 02/16/2005

XILINX, INC  
ATTN: LEGAL DEPARTMENT  
2100 LOGIC DR  
SAN JOSE, CA 95124

EXAMINER

CHANG, DANIEL D

ART UNIT	PAPER NUMBER
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2819

DATE MAILED: 02/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

10/666,669

Applicant(s)

TUAN ET AL.

Examiner

Daniel D. Chang

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 24 January 2005.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 26-37 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 26-37 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 19 September 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>9/19/03, 8/3/04</u> . | 6) <input type="checkbox"/> Other: _____  |

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***Election/Restrictions***

Applicant's election of Group II, claims 26-37 in the reply filed on January 24, 2005 is acknowledged.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 26-28 and 32-34 are rejected under 35 U.S.C. 102(e) as being anticipated by Sani et al. (US 2003/0218478 A1, hereinafter Sani).

Regarding claims 26 and 33, Sani discloses, at least in Fig. 2, a programmable logic device (paragraph 0048) comprising:

a first voltage supply terminal (206 VDD) configured to receive a first supply voltage;  
a plurality of programmable logic blocks (210), each programmable logic block comprising one or more resources (inherent for PLD or FPGA) of the programmable logic device; and

a plurality of first switch elements (or voltage regulators 212), wherein each first switch element is coupled between one of the programmable logic blocks and the first voltage supply terminal.

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Regarding claim 27, Sani discloses, at least in Fig. 2, a second voltage supply terminal (208 GND) configured to receive a second supply voltage; and a plurality of second switch elements (214), wherein each second switch element is coupled between one of the programmable logic blocks and the second voltage supply terminal.

Regarding claims 28 and 34, Sani discloses, at least in Fig. 2, a control circuit (inherent circuit that generates SL and /SL signals) coupled to the plurality of first switch elements, wherein the control circuit is configured to provide a plurality of control signals (SL) for controlling the plurality of first switch elements or voltage regulators.

Regarding claim 32, Sani discloses, at least in Fig. 2, that each first switch element comprises a transistor (212).

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 29-31 and 35-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sani in view of Goetting et al. (US 5,958,026, hereinafter Goetting).

The teachings of Sani have been discussed above.

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Sani does not teach that the control circuit (inherent circuit coupled to SL and /SL) comprises a plurality of configuration memory cells or a plurality of user control terminals to turn on and off transistors.

However, Goetting teaches a control circuit (110-117) having a plurality of configuration memory cells (120-127) and receiving a plurality of user control terminals (PUP, PDNB, EN) that turns on and off transistors (100-107).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of applicant's invention to have provided the circuit of Sani with control circuit as taught by Goetting in order to provide configuration data and enable/disable signal to the control circuit.

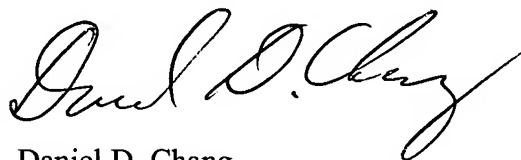
### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel D. Chang whose telephone number is (571) 272-1801. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael J. Tokar can be reached on (571) 272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Daniel D. Chang  
Primary Examiner  
Art Unit 2819

dc

**DANIEL CHANG  
PRIMARY EXAMINER**